What is claimed is:

1. An FDTS/DF equalizer using absolute value calculation comprising:

a feed-forward filter receiving and filtering a sampled signal;

a feed-back filter filtering a restored data;

a subtractor obtaining a difference between signals respectively filtered by the feed-forward filter and the feed-back filter; and

a detector means receiving the subtracted signal and detecting a data using absolute value calculation.

2. The equalizer of claim 1, wherein the feed-forward filter changes the sampled signal to a causal signal.

3. The equalizer of claim 1, wherein the feed-back filter removes an intersymbol interference of the causal signal.

4. The equalizer of claim 1, wherein the detector means comprises:

a plurality of branch metric calculating means obtaining an error between the subtracted signal and a reference signal;

an adder adding the values outputted from the plurality of branch metric calculating means;

a path metric memory means storing the added value;

a minimum value calculating means calculating a minimum value of the accumulated values; and

a comparator comparing the minimum values and outputting the most minimum value.

5. The equalizer of claim 4, wherein the plurality of branch metric calculating means are sequentially delayed as deep as τ from '0', respectively.

6. The equalizer of claim 4, wherein the branch metric operating means comprises:

a plurality of absolute value calculating means obtaining an absolute value of the difference between the subtracted value and the reference signal; and

a demultiplexer demultiplexing the signal outputted from the absolute value calculating means.

7. An FDTS/DF equalizer using absolute value calculation of a system restoring a data signal passing through a channel comprising:

an equalizer making a sampled data signal to be a causal signal and removing an intersymbol interference of the causal signal; and

a detector detecting an original data from the signal without the intersymbol interference by using absolute value calculation.

8. The equalizer of claim 7, wherein the detector comprises:

a plurality of branch metric calculating means obtaining an error between the subtracted signal and the reference signal;

an adder for adding values outputted from the plurality of branch metric calculating means;

a path metric memory means storing the added value;

a minimum value calculating means calculating a minimum value of the accumulated values; and

a comparator comparing the minimum values and outputting the most minimum value.

9. The equalizer of claim 8, wherein the plurality of branch metric calculating means are sequentially delayed as deep as τ from '0', respectively.

10. The equalizer of claim 8, wherein the branch metric calculating means comprises:

a plurality of absolute value calculating means obtaining an absolute value of a difference between the subtracted value and the reference signal; and

a demultiplexer demultiplexing a signal outputted from the absolute value calculating means.

11. A data restoring method of an FDTS/DF equalizer using absolute value calculation comprising the steps of:

obtaining a difference between signals respectively filtered by a feed-forward filter and a feed-back filter;

computing an error through absolute value calculation between the signal difference and a reference signal;

delaying the error as deep as τ and adding them;

storing the added results; and

obtaining a minimum value of the stored error values and obtaining a path

according to the minimum value.

12. The method of claim 11, wherein, in the path obtaining step, only the branch metric containing a selected path is left while the remaining branch metrics are discarded.